This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

Claims 1-17(canceled).

18(currently amended). A method of fabricating a cell transistor, comprising the steps of:

forming a groove recessed into a semiconductor substrate;

forming a source region in said semiconductor substrate, wherein said source region overlaps with said groove, so that said source region covers said groove entirely;

sequentially forming a gate electrode by laminating and patterning a gate insulating layer, a floating gate, an inter-gate layer, and a control gate on said semiconductor substrate; and

forming a drain region in said semiconductor substrate.

19(previously presented). The method of claim 18, wherein the step of forming the groove includes the steps of:

sequentially forming a buffer layer and an etching mask layer on said semiconductor substrate;

patterning said etching mask layer such that a portion of said buffer layer is exposed;

forming a spacer on inner walls of said patterned etching mask;

patterning said buffer layer by using said spacer as an etching mask; and

forming said groove, recessed into the semiconductor substrate, by using said patterned buffer layer as an etching mask.

20(previously presented). The method of claim 18, further comprising the step of:

removing the buffer layer after the step of forming said source region.

21(previously presented). The method of claim 19, wherein said buffer layer and said etching mask layer are respectively made of first and second insulation materials, wherein said first and said second insulation material have different etching selectivities.

22(previously presented). The method of claim 18, wherein said groove is formed by a dry etching.

23(previously presented). The method of claim 18, wherein said groove is formed by a wet etching.

24(previously presented). The method of claim 18, wherein said groove is a V-shaped groove, a U-shaped groove, or a rectangular groove.

25(previously presented). The method of claim 18, wherein said groove has a depth of about 0.1 μm to about 0.2 μm.

26(previously presented). The method of claim 18, wherein said groove has a width of about 0.1 μm to about 0.2 μm.

27(previously presented). The method of claim 18, wherein said floating gate overlaps with said source region at a width of about 0.4 μm to about 0.6 μm.